Attorney Docket No. [redacted]*4314*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

Title: METHOD FOR EVALUATING ANOMALIES IN A SEMICONDUCTOR MANUFACTURING PROCESS

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METHOD FOR EVALUATING ANOMALIES IN A SEMICONDUCTOR MANUFACTURING PROCESS

FIELD OF THE INVENTION

This invention relates, in general, to semiconductor manufacturing processes and, more particularly, to identifying process signatures of the semiconductor manufacturing process.

BACKGROUND OF THE INVENTION

It is well known that integrated circuits and discrete semiconductor devices are manufactured using a series of process steps. A typical semiconductor process flow may involve more than one hundred process steps including processes such as lithography, etching, doping, oxidation, planarization, metallization, passivation, and cleaning, among others. Although the process steps for manufacturing integrated circuits have been well characterized, a significant number of defects still appear on the semiconductor wafers. Events capable of causing these defects include, but are not limited to, particle contamination, scratching, polishing anomalies, wafer spinning processes, watermarks, particle stains, and micro-scratching. Making matters worse, semiconductor manufacturers are increasing the density of devices per die and increasing the size of the wafers to increase the number of die per wafer. Thus, a few defects on a wafer can significantly decrease the die yield on the wafer.

Hence, semiconductor manufacturers have incorporated inspection techniques using optical image devices capable of discerning unique defect patterns on a wafer surface, commonly referred to as defect spatial signatures. FIG. 1 is a wafer map 10 showing random defects on a semiconductor wafer. It should be noted that the distinguishing feature of a wafer map having random defects is the absence of any type of pattern or any defect spatial signatures. A problem with random defects is that finding the cause of the defects is extremely difficult. FIG. 2 is a wafer map 15 of a semiconductor wafer having a defect spatial signature caused by, for example, a wafer spinning process. Although the optical image devices allow engineers to view the defect spatial signatures on a wafer, it is

difficult for engineers to remember all the types of defect spatial signatures they have seen and associate a particular signature with a particular process step or piece of process equipment.

Accordingly, what is needed is a method to enable engineers to review a defect spatial signature and associate the signature with a specific process step or piece of process equipment.

SUMMARY OF THE INVENTION

The present invention satisfies the foregoing need by providing a method for performing defect spatial signature analysis. In a preferred embodiment, defect information and the associated identification information are stored in a relational database. A defect spatial signature for a newly inspected wafer is generated and the relational database is searched to determine if the new defect spatial signature matches any of the defect spatial signatures in the relational database. If a match occurs, the engineers are notified. The defect information and its associated wafer identification information are stored in the relational database.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures in which like references designate like elements and in which:

FIG. 1 is a wafer map lacking a defect spatial signature;

FIG. 2 is a wafer map illustrating a defect spatial signature;

FIG. 3 is a flow chart of a process for performing defect spatial signature analysis in accordance with an embodiment of the present invention; and

FIG. 4 is a wafer map illustrating a defect spatial signature having a clustering boundary.

DETAILED DESCRIPTION

The present invention provides a method for determining whether a particular defect on a semiconductor wafer has been encountered previously. These defects are anomalies caused by anomalous events in the semiconductor manufacturing process. Examples of process steps that can cause defects having defect spatial signatures, include, but are not limited to, particle contamination, mechanical surface damage, wafer spinning processes, scratching, and polishing. This method provides for electronically searching a database to determine if a spatial signature has occurred before and, if so, notifying an engineer. FIG. 3 is a flow chart of a process for performing defect spatial analysis in accordance with an embodiment of the present invention. In a beginning step identified by reference number 21, an electronic wafer map for a first wafer having a defect associated therewith is generated. In a next step (reference number 23), the electronic wafer map of the first wafer is partitioned into defect regions or areas, i.e., the defects are clustered using mathematical clustering techniques or using a stylus and a pad. Briefly referring to FIG. 4, a wafer map 16 of a defect spatial signature having a cluster boundary 17 is illustrated. The clustering is accomplished using a stylus and pad coupled to a computer system displaying an image of the defect spatial signature. By way of example, the defects are caused at a furnace operation in a semiconductor manufacturing process. The wafer map is stored in a relational database (reference number 25), such that the relationship of the defects to each other are stored in a row and column format.

An electronic wafer map of a second wafer is generated (reference number 27). The wafer map of the first wafer is reconstructed from the relational database (reference number 29) and the wafer maps of the two wafers are electronically analyzed to determine if the wafer map of the first wafer correlates to that of the second wafer within a predetermined confidence level (reference number 31). If a match within the predetermined confidence level occurs, then the computer reports that a match has been encountered. The engineer is notified and can then review the process history of the first wafer with that of the second wafer to discover at which step in the process the defect occurred. Using this information, the engineer can take appropriate corrective action to prevent the defect from occurring again (reference number 33).

The electronic wafer map of the second wafer is partitioned into defect areas, which are stored in the relational database (reference number 35), such that the

relationship of the defects within the wafer are stored in a row and column format. Similar to the first wafer, wafer identification information of the second wafer is also stored in the computer database. The relational database now includes wafer defect information of the first two wafers and their associated identification information.

As each new wafer map is generated, it is compared with the reconstructed wafer maps present in the relational database to determine if a match exists between the new wafer map and any wafer map existing in the computer database. If a match exists, the engineer is notified and can take an appropriate action. The new wafer map is partitioned into defect areas which, along with its associated wafer identification information, are stored in the relational database (reference number 37).

By now it should be appreciated that a method has been provided for performing defect spatial analysis that is fast, accurate, and economical. The method allows an engineer to sift through large amounts of data in diagnosing process problems without having to rely on their own memories of past occurrences of wafer defects. A particular advantage of the present invention is that it eliminates steps such as categorizing and correlating defect data, thereby saving time for the engineer and the costly step of writing software programs capable of performing the categorization and/or correlation. Thus, the data in the relational database is uncategorized and uncorrelated. Another advantage of the present invention is that it removes the variability inherent in manually analyzing defect spatial signatures, i.e., the present method mitigates the differences in interpretation between two or more engineers. The present method also improves the process flow by providing a means for quickly identifying the causes of defects, thereby improving wafer throughput.

Although certain preferred embodiments and methods have been disclosed herein, it will be apparent from the foregoing disclosure to those skilled in the art that variations and modifications of such embodiments and methods may be made without departing from the spirit and scope of the invention. It is intended that the invention shall be limited only to the extent required by the appended claims and the rules and principles of applicable law.